ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device is provided that enables testing of an optimum test unit in a memory macro under optimum test conditions when testing the memory macro provided in the semiconductor integrated circuit device. An inner bus IB is connected to a self-test circuit, and a self-test is performed on each physical region, which is a basic region in a physical address space of a memory cell array 11. The test is performed constantly with a physical region as a basic unit and redundancy remedy of each basic unit can be performed, irrespective of an outer bus OB set in a logical address space under the control of a logical macro. At the time of the self-test, a memory macro 1 can be tested using an internal clock signal iCLK or second-latency-value information L1 that is optimum for the memory macro. Moreover, output latency of the result of detection of a defective memory cell based on the test can be adjusted in accordance with a signal propagation delay time due to a wiring load in the signal route.